What is claimed is:

1. A memory device comprising:

a dynamic random access memory capacitor that provides a dynamic mode of operation; and

a nitride read only memory (NROM) transistor that provides a repressed non-volatile random access memory mode of operation, the NROM transistor coupled between the capacitor and a data line and acting as a transfer gate for the capacitor.

2. The memory device of claim 1 wherein the NROM transistor is coupled to other NROM transistors by a word line coupled to a control gate of each NROM transistor.

3. The memory device of claim 1 wherein the capacitor is coupled between ground and one of either a source or drain region of the NROM transistor.

4. The memory device of claim 2 wherein the NROM transfers data from the capacitor to the data line when the word line is biased at a voltage that is greater than a threshold voltage of the transistor.

5. The memory device of claim 1 wherein a charge stored in the transistor affects a transfer rate of data from the capacitor to the data line.

6. The memory device of claim 2 wherein the capacitor is read when a voltage within a normal operating range of the transistor is applied to the word line.

7. The memory device of claim 6 wherein the voltage is 3.0 volts.

8. A memory device comprising:

a plurality of source/drain regions formed in a substrate, a first source/drain region coupled to a bit line;

a dynamic random access memory capacitor that provides a dynamic data storage mode of operation, the capacitor coupled to a second source/drain region;

a gate insulator layer formed on the substrate substantially between the plurality of source/drain regions, the gate insulator layer comprised of a composite oxide-nitride-oxide structure; and

a control gate formed on the gate insulator layer, the control gate coupled to a word line.

9. The memory device of claim 8 wherein the plurality of source/drain regions are n+ doped regions in the substrate that is comprised of a p-type conductivity material.

10. The memory device of claim 8 wherein the plurality of source/drain regions, the gate insulator, and the control gate form a nitride read only memory (NROM) transistor that provides a repressed non-volatile random access memory mode of operation.

11. The memory device of claim 8 and further including a sense amplifier coupled to the bit line such that a difference in a rate of charge transfer determined by the sense amplifier determines a presence or absence of a stored charge on the oxide-nitride-oxide structure.

12. The memory device of claim 8 wherein the control gate is comprised of a polysilicon material.

13. An array of memory devices comprising:

a plurality of sense amplifiers, each amplifier coupled to a different bit line that can contain data from a column of the array of memory devices;

a plurality of nitride read only memory (NROM) transistors that provide a repressed non-volatile random access memory mode of operation, the NROM transistors each comprising a control gate formed on a substrate between a first and a second source/drain region, the first source/drain region coupled to a bit line;

a plurality of dynamic random access memory capacitors that provide a dynamic mode of data storage, each capacitor coupled to the second source/drain region; and

a plurality of word lines, each word line coupling the control gates of a row of the plurality of NROM transistors.

14. The array of claim 13 wherein the NROM transistor can contain data independent of a state of the capacitor.

15. The array of claim 13 wherein the NROM transistor is a shadow memory for the capacitor such that it contains data equivalent to data stored in the capacitor.

16. An electronic system comprising

a processor that generates control signals; and

a memory device coupled to the processor and operating in response to the control signals, the device comprising:

a dynamic random access memory capacitor that provides a dynamic mode of operation; and

a nitride read only memory (NROM) transistor that provides a repressed non-volatile random access memory mode of operation, the NROM transistor coupled between the capacitor and a data line and acting as a transfer gate for the capacitor, the transistor comprising a control gate and a data storage layer.

17. The method of claim 16 wherein the NROM transistor is used as a shadow memory for the dynamic random access memory capacitor such that data from the capacitor is written to the NROM transistor upon a power-down condition of the system.

18. The system of claim 16 and further including a sense amplifier coupled to the data line such that the sense amplifier can

19. The system of claim 16 wherein data is written into the capacitor when the control gate is biased at a first potential and data is written into the transistor's data storage layer when the control gate is biased at a second potential that is higher than the first potential.

20. A method for reading a memory device comprising a dynamic read only memory capacitor coupled to first source/drain region of a non-volatile, nitride read only memory transistor, the transistor having a control gate coupled to a word line and a second source/drain region coupled to a bit line, the method comprising:

determining if the memory device is being accessed as a dynamic read only memory or as a non-volatile memory in response to a voltage level applied to the word line; and

if the memory device is accessed as a non-volatile memory, determining a current difference through the transistor to determine a state of the transistor.

21. The method of claim 20 wherein a sense amplifier coupled to the bit line is used to determine the current difference by measuring differences in response time that changes in response to differences in a threshold voltage of the transistor.

22. A method for reading a memory device comprising a dynamic read only memory capacitor coupled to first source/drain region of a non-volatile, nitride read only memory transistor, the transistor having a control gate coupled to a word line and a

second source/drain region coupled to a bit line that is coupled to a sense amplifier, the method comprising:

determining if the memory device is being accessed as a dynamic read only memory or as a non-volatile memory in response to a voltage level applied to the word line;

if the memory device is accessed as a non-volatile memory, charging the capacitor; and

determining a charge state of the transistor by measuring a plurality of currents supplied by the transistor through the bit line, each at a different gate voltage, and determining a response time of the sense amplifier at each gate voltage.

23. The method of claim 22 and further including reading the capacitor in response to the determination that the memory is being accessed as a dynamic read only memory.